4x8 RF Switch Matrix

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Current document represents technical data for solid state 4x8 RF switch matrix.

Device enables very high test equipment utilization by switching RF routes between four (4) instrument and eight(8) Device Under Test (DUT).

Features and advantages:

- Enables reducing test time per DUT by high speed RF route switching between multiply test instruments and DUT's.
- Maintenance free, no limitation for switching cycles
- Based on high-end UltraCMOS technology
- Broadband coverage from 1MHz up to 6.0 GHz
- High switching speed
- High isolation and low VSWR
- Unused RF ports are internally terminated into 50Ω
- RF and control routes are ESD protected
- Enable 3,3V or 5V control

Absolute maximum ratings:

Parameter	Minimum	Maximum
Frequency range	10MHz	6GHz
Operating voltage,Vdd	3.2V	5.5V
Control voltage, Vctrl	3.2V	5.5V
RF input power for active		+27 dBm @10-50MHz
RF route		+30 dBm @50-400MHz
		+34 dBm @0.4-6GHz
RF input power for unused		+24 dBm @10MHz-6GHz
port (to internal termination)		
Hot switching: allowed but not		+24dBm max
recommended		
Operating tem.	-10°C	+65°C

Technical specifications:

Parameter	10MHz-0.7GHz	0.7-4.0 GHz	4.0-6.0GHz
Input impedance	50 ohm		
Insertion loss max.	5.5 dB	8.0 dB	9.0dB
Return Loss min.	17dB	20dB	15dB
Isolation between used and unused port	>50 dB	>40 dB	>35 dB
Input 1dB compression, typ	+26 dBm	+33 dBm	+33 dBm
Input IP3, typ	+56dBm	+60dBm	+60dBm
Switching time	<20µsec		
RF connectors, Port A1 - A4	4xN-female		
RF connectors, Port B1 – B8	8x SMA-female		
CTRL connector	DIN 41651, 50-pin PCB angled male connector		
DC connector	Phoenix contact, 3-pin PCB angled connector, 3,5mm pitch		
Case dimensions WxDxH (without connectors)	120x150x22mm		





Control and DC connection diagram



8x4 Matrix control description

Switch matrix consists of two RF relay arrays A of size 4 and B of size 8.

Relays of arrays A and B must be addressed in such a way that signal path of relays pointed to each other must meet in between. For example if port A[2] is to be connected to port B[5], then relay cluster of port A[2] must address destination of port B[5] and accordingly relays of port B[5] must address port A[2]. If we primary select port A destination then address of the port B could be calculated from expression: for i := 0 to 3 do

begin

Bsel [Asel [I]] := i; end;

where Asel and Bsel are selection addresses of port relay matrixes A and B accordingly.

There must be noted that with asymmetric matrix 4 x 8, four of B ports will remain unconnected, but still must (are) be pointed to some of the A ports. Careful selection of this destination could improve isolation of valid connections. Since destination range of port A is 0 to 7 then 3 bit address is applied to the each of 4 A port relay matrixes. Control lines of A ports are connected as:

Accordingly each of 8 ports B relay matrixes address one of 4 ports A and each has 2 bit address connected as:

B[0].1 – pin 39
B[1].1 – pin 37
B[2].1 – pin 35
B[3].1 – pin 33
B[4].1 – pin 47
B[5].1 – pin 45
B[6].1 – pin 43
B[7].1 – pin 41

Pins 49 and 50 are connected to the common ground.

There are LVC technology buffers on each connector input pin to protect relays from static electricity and incorrect input voltages.

Better solution would be internal controller performing all needed address calculation tasks and interfaced from outside just by USB connector. In this case the power could be also derived from USB line.











